

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Norikatsu TAKAURA et al.

Appln. No.:

Filed: Herewith

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND PRODUCTION  
METHOD THEREOF

\* \* \*

INFORMATION DISCLOSURE STATEMENT

Commissioner of Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

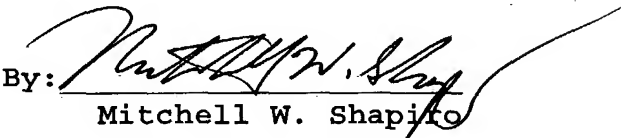
Sir:

Applicants wish to make of record the documents cited  
in prior Application No. 10/164,008 filed June 7, 2002,  
whether cited by Applicants or by the Patent Office. The  
documents are listed on the attached Form PTO-1449.

Respectfully submitted,

MWS:jab

Miles & Stockbridge P.C.  
1751 Pinnacle Drive, Suite 500  
McLean, Virginia 22102-3833  
(703) 903-9000  
July 10, 2003

By:   
Mitchell W. Shapiro  
Reg. No. 31,568

FORM PTO-1449				Atty. Docket No. XA-9689A		Appln. No.	
<u>LIST OF DOCUMENTS CITED BY APPLICANT</u>				Applicant Norikatsu TAKAURA et al.			
				Filing Date Herewith		Group	
U.S. PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Name	Class	Sub-class	Filing Date
	AA	6,153,490	11-2000	Xing et al.	438	396	
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
FOREIGN PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
	AL	2000-174225	6/00	Japan			Abstract
	AM	09-036318A	02/97	Japan			
	AN	04-058556A	02/92	Japan			
	AO	02-214155A	09/90	Japan			
	AP						
	AQ						
	AR						
	AS						
OTHER (including author, title, date, pertinent pages, etc.)							
	AT	Kistler, N. et al., "Symmetric CMOS in Fully-Depleted Silicon-On-Insulator Using P+-Polycrystalline Si-Ge Gate Electrodes," Dec. 1993, IEDM 93, pp. 727-730.					
Examiner				Date Considered			
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.							